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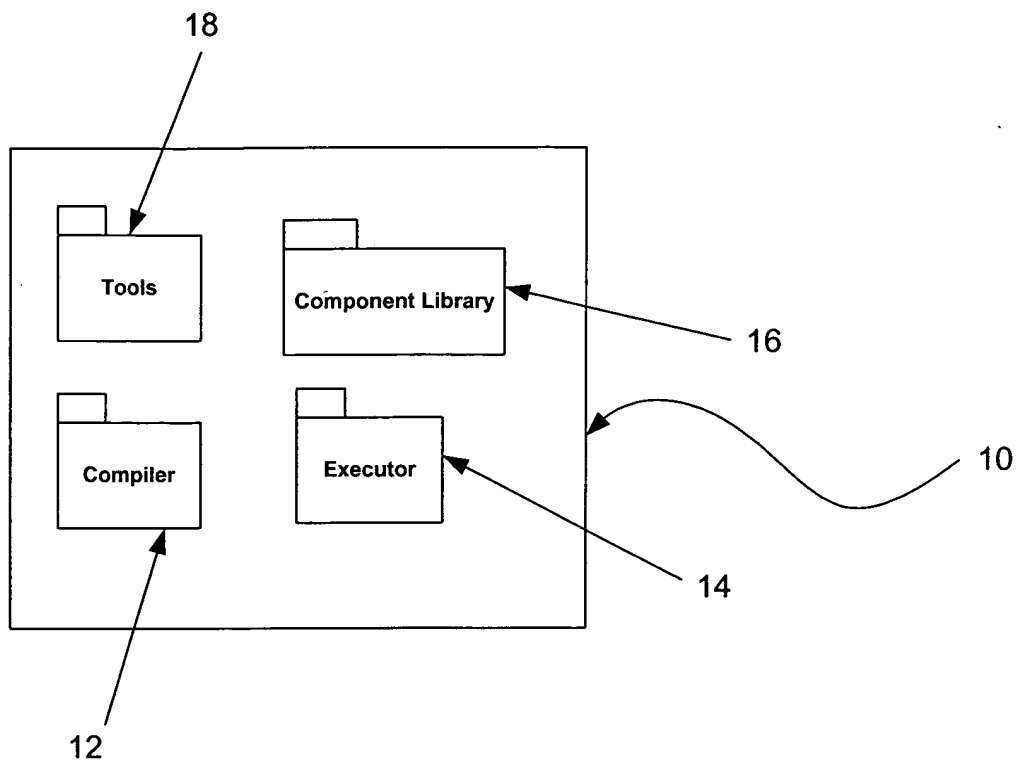
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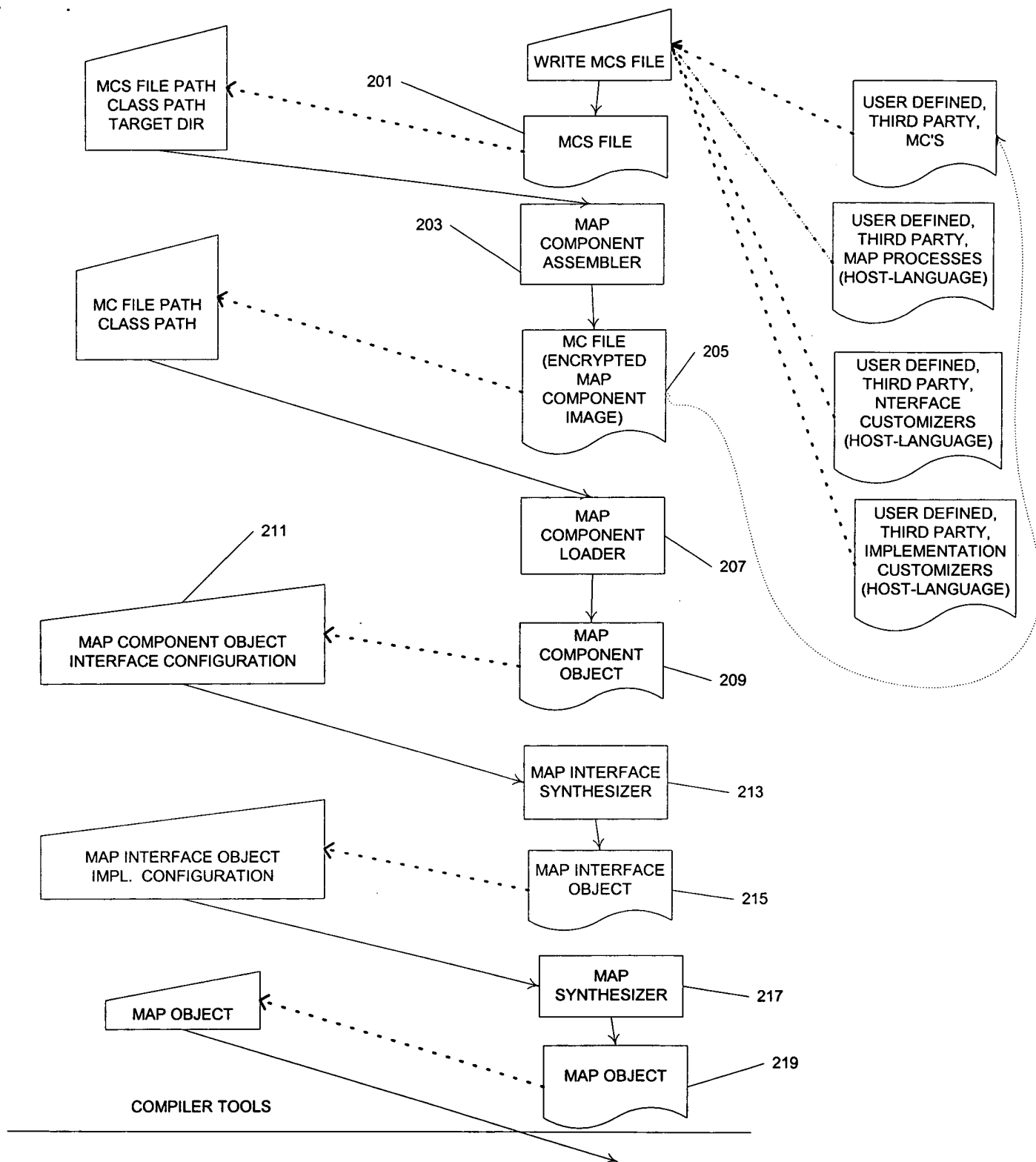
*IMAGE CUT OFF FIG. 11*

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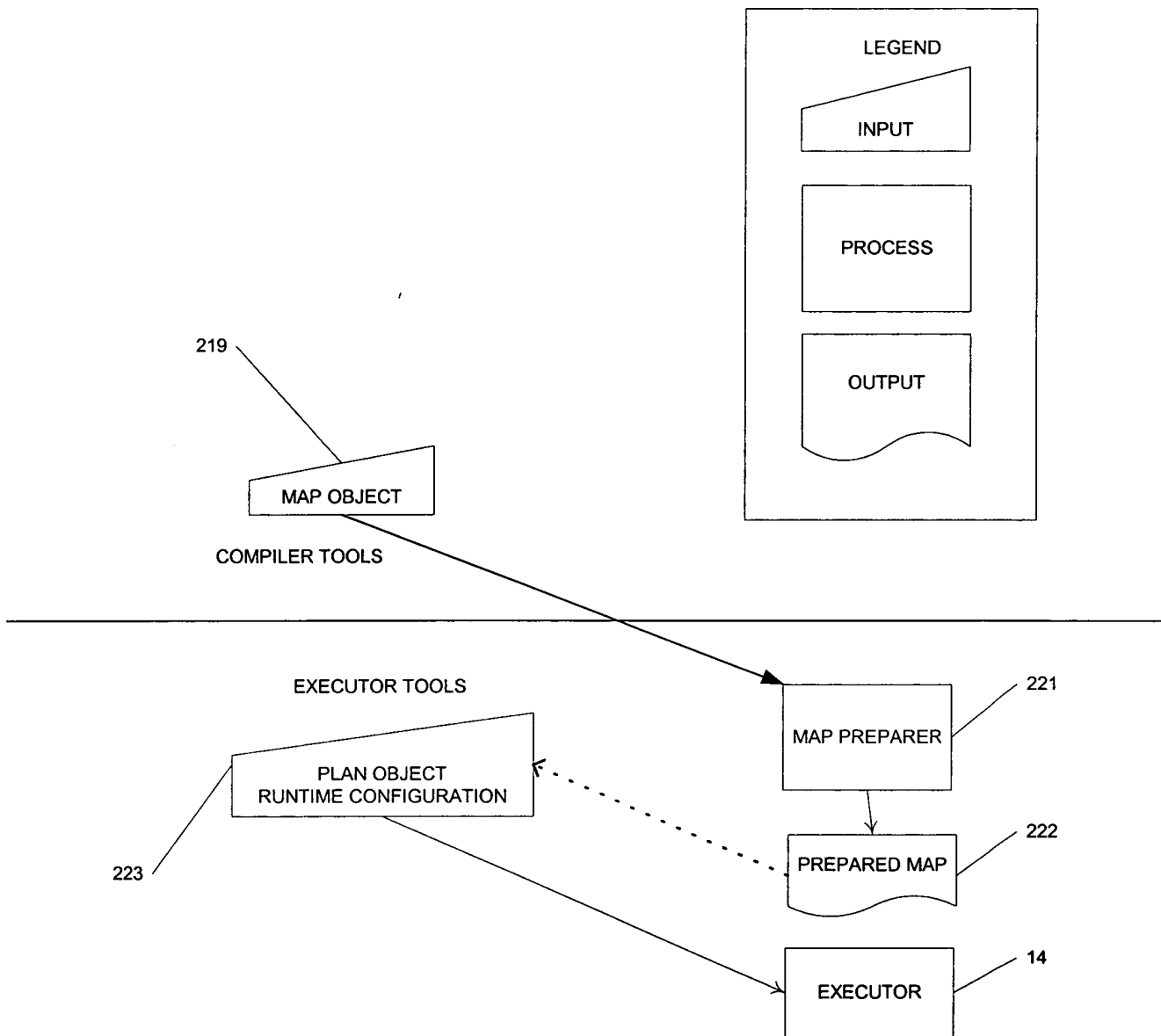
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**Fig. 1**

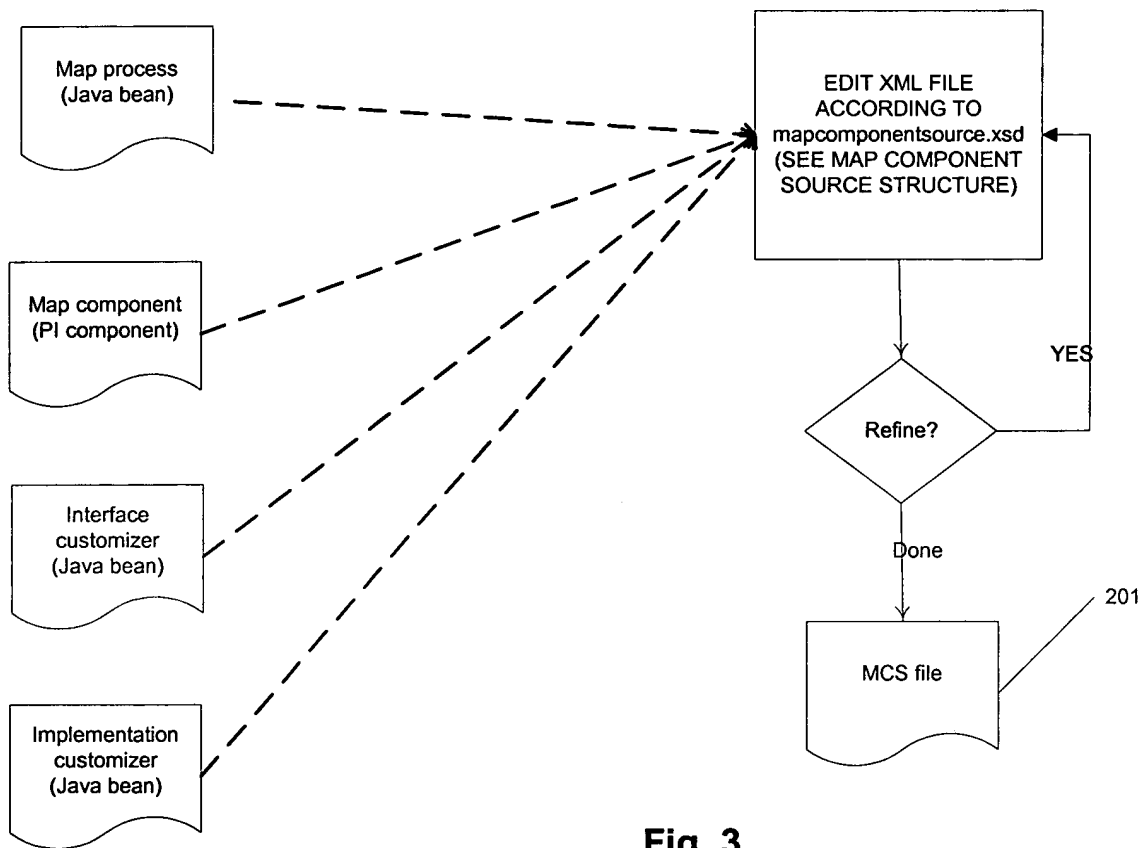


**Fig. 2A**



**Fig. 2B**

# MAP COMPONENT SOURCE CREATION



**Fig. 3**

Fig. 4

201

## ***INTERFACE***

DOCUMENTATION

INTERFACE PROPERTY LIST  
IMPLEMENTATION PROPERTY LIST  
RUNTIME PROPERTY LIST

PORT DECLARATION LIST ...

CUSTOMIZER DECLARATION AND  
CONFIGURATION

## ***IMPLEMENTATION***

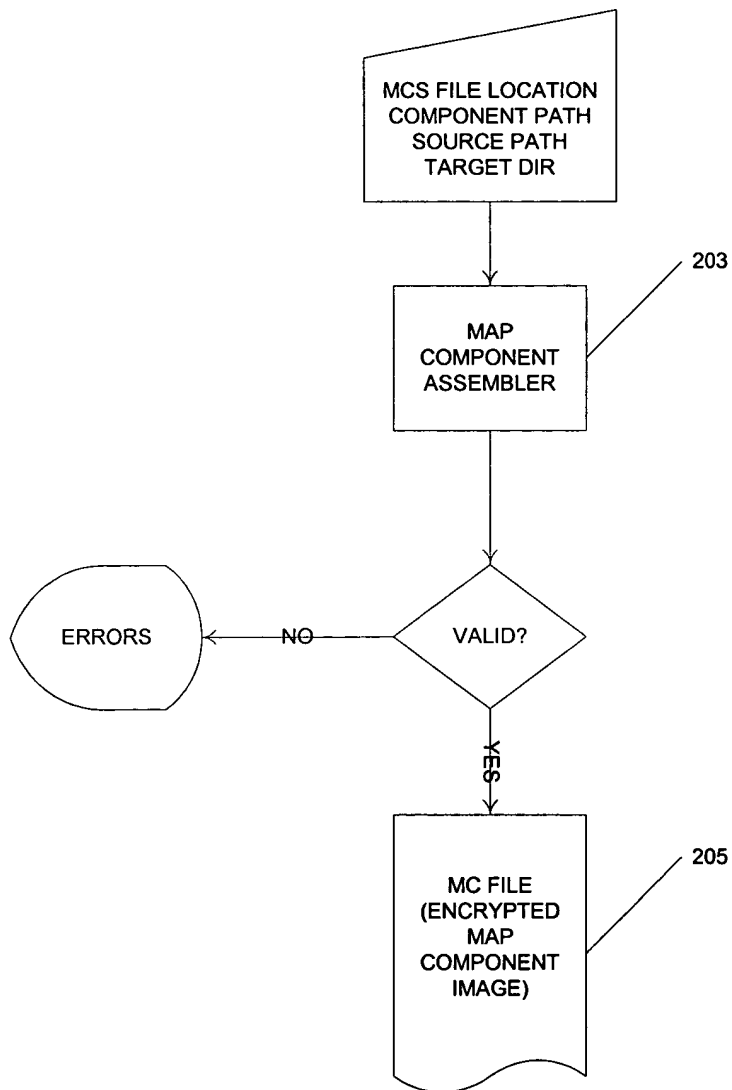
INTERNAL MAP COMPONENT INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

INTERNAL MAP PROCESS INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

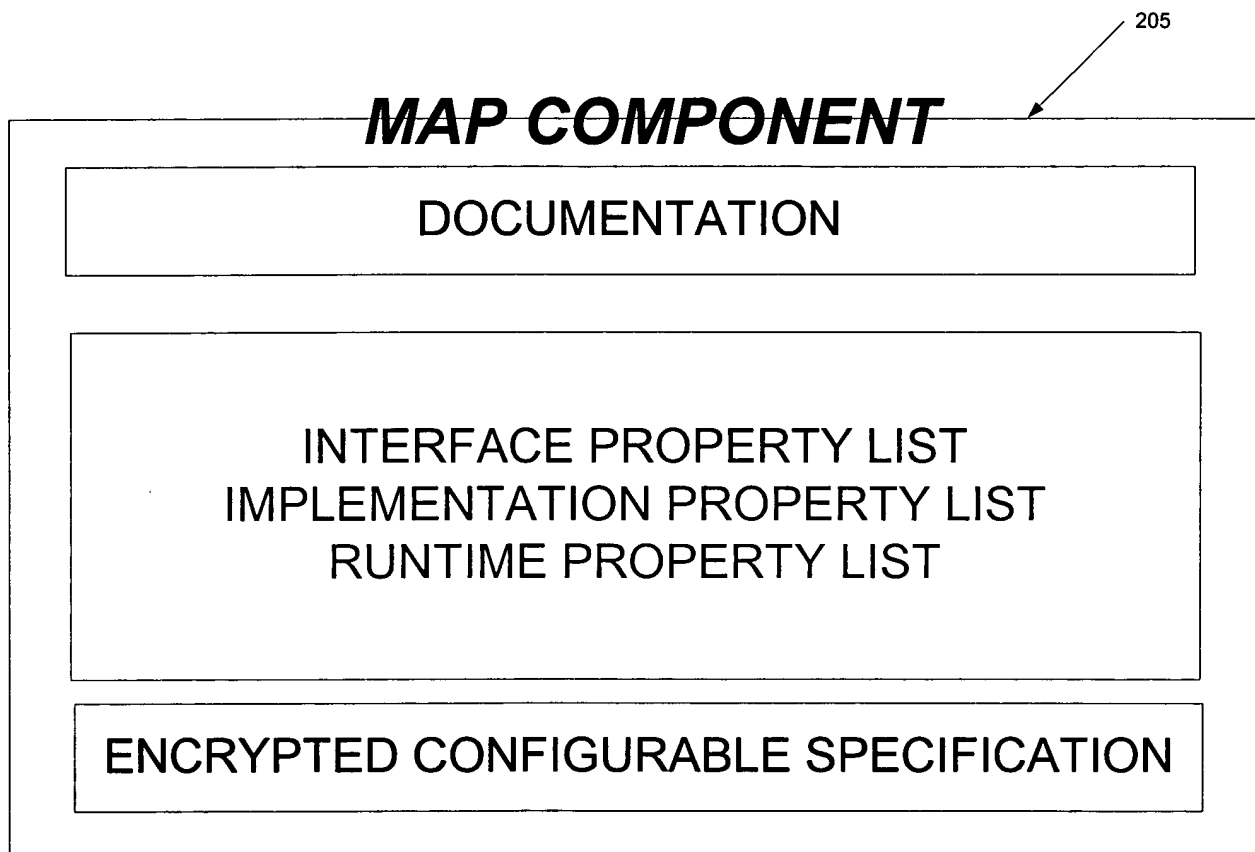
PORT TO PORT LINK LIST...

CUSTOMIZER DECLARATION AND  
CONFIGURATION

# MAP COMPONENT ASSEMBLY PROCESS



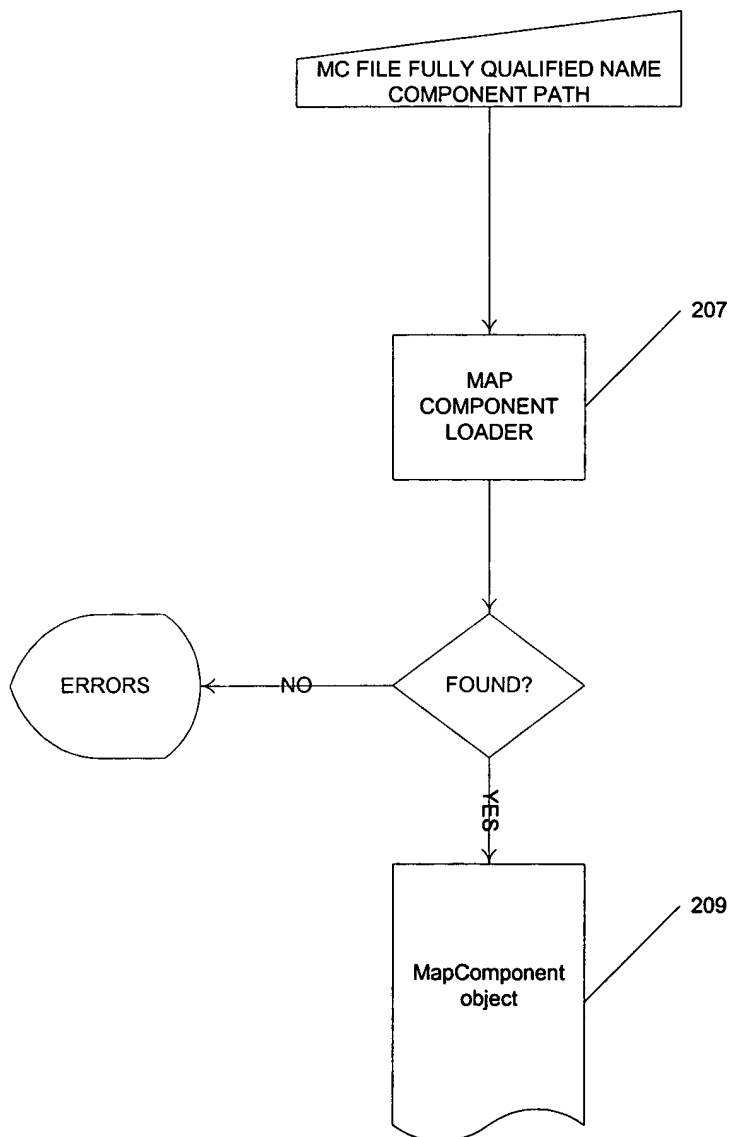
**Fig. 5**



**Fig. 6**

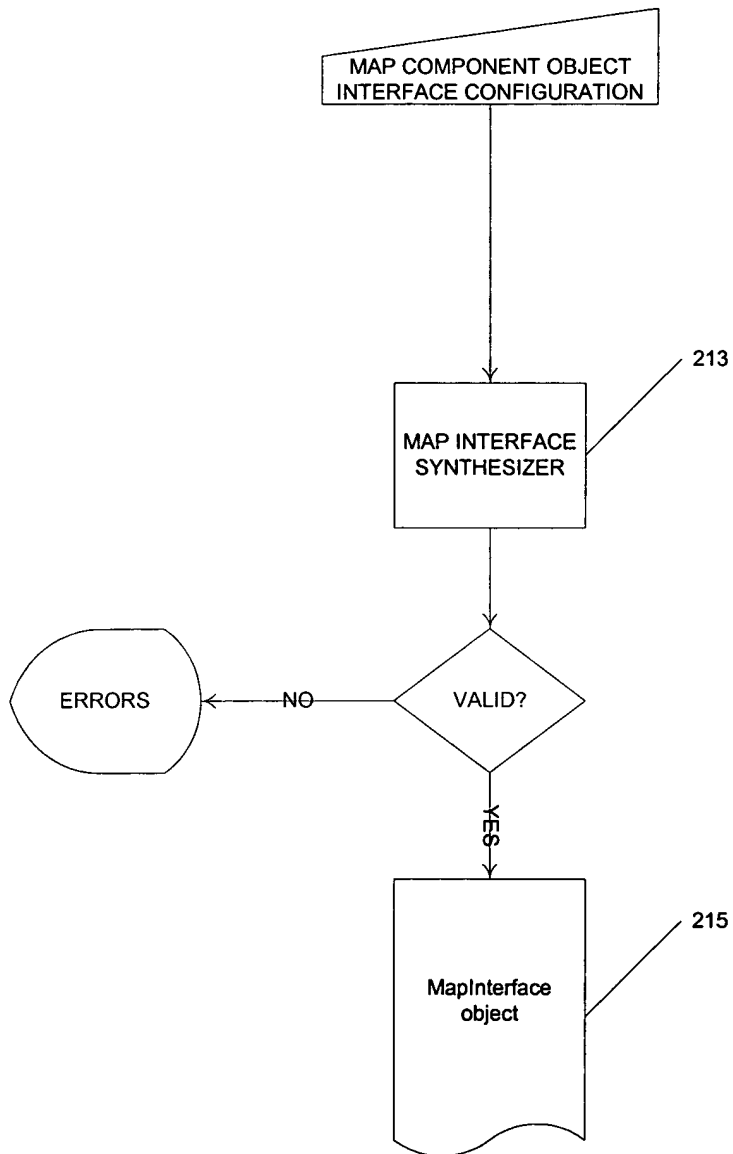


# MAP COMPONENT LOADING

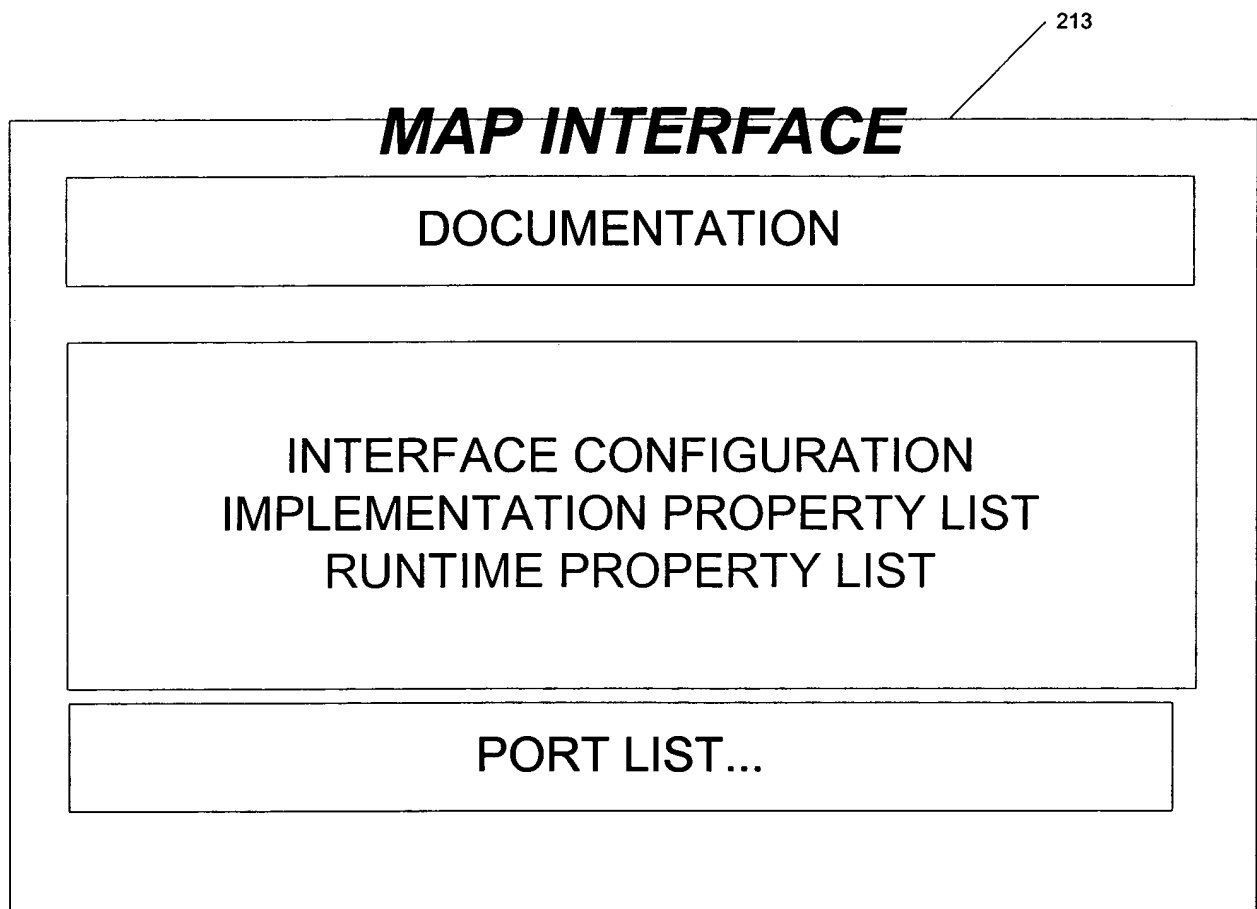


**Fig. 7**

# MAP INTERFACE SYNTHESIS

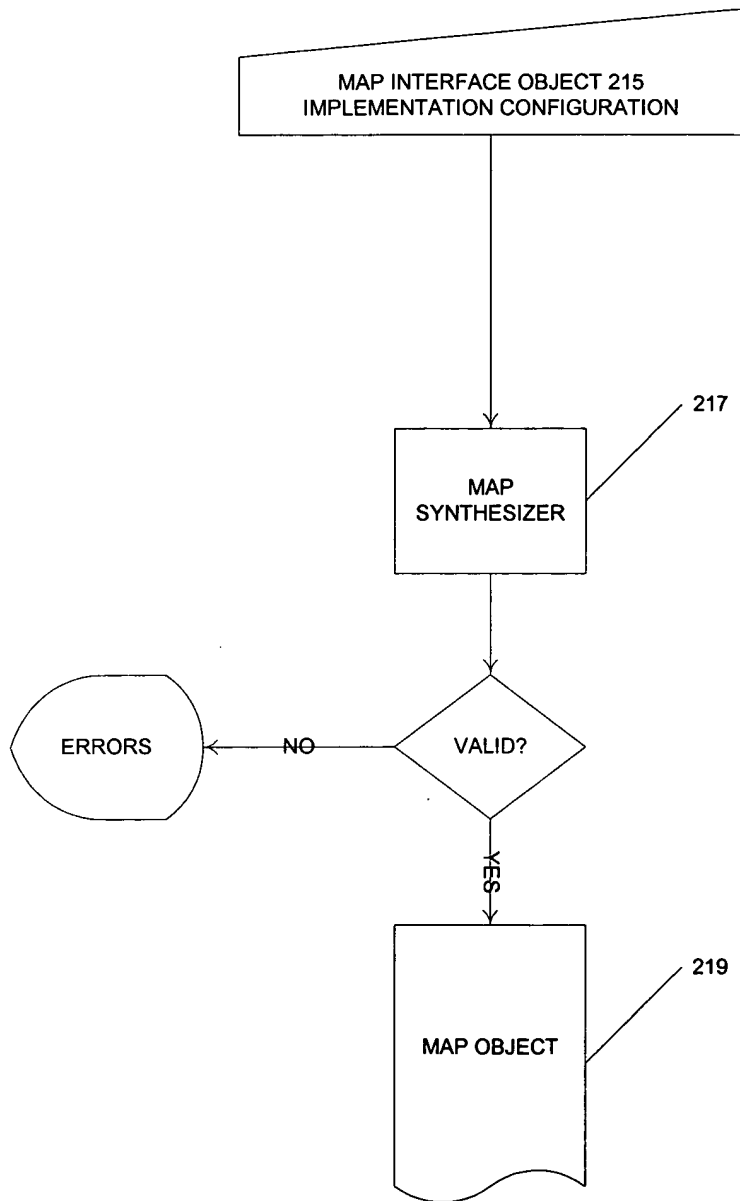


**Fig. 8**



**Fig. 9**

# MAP SYNTHESIS



**Fig. 10**

**MAP**

DOCUMENTATION

INTERFACE CONFIGURATION  
IMPLEMENTATION CONFIGURATION  
RUNTIME PROPERTY LIST

**INTERFACE**

PORT DECLARATION LIST ...

**IMPLEMENTATION (if open)**

INTERNAL MAP COMPONENT INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

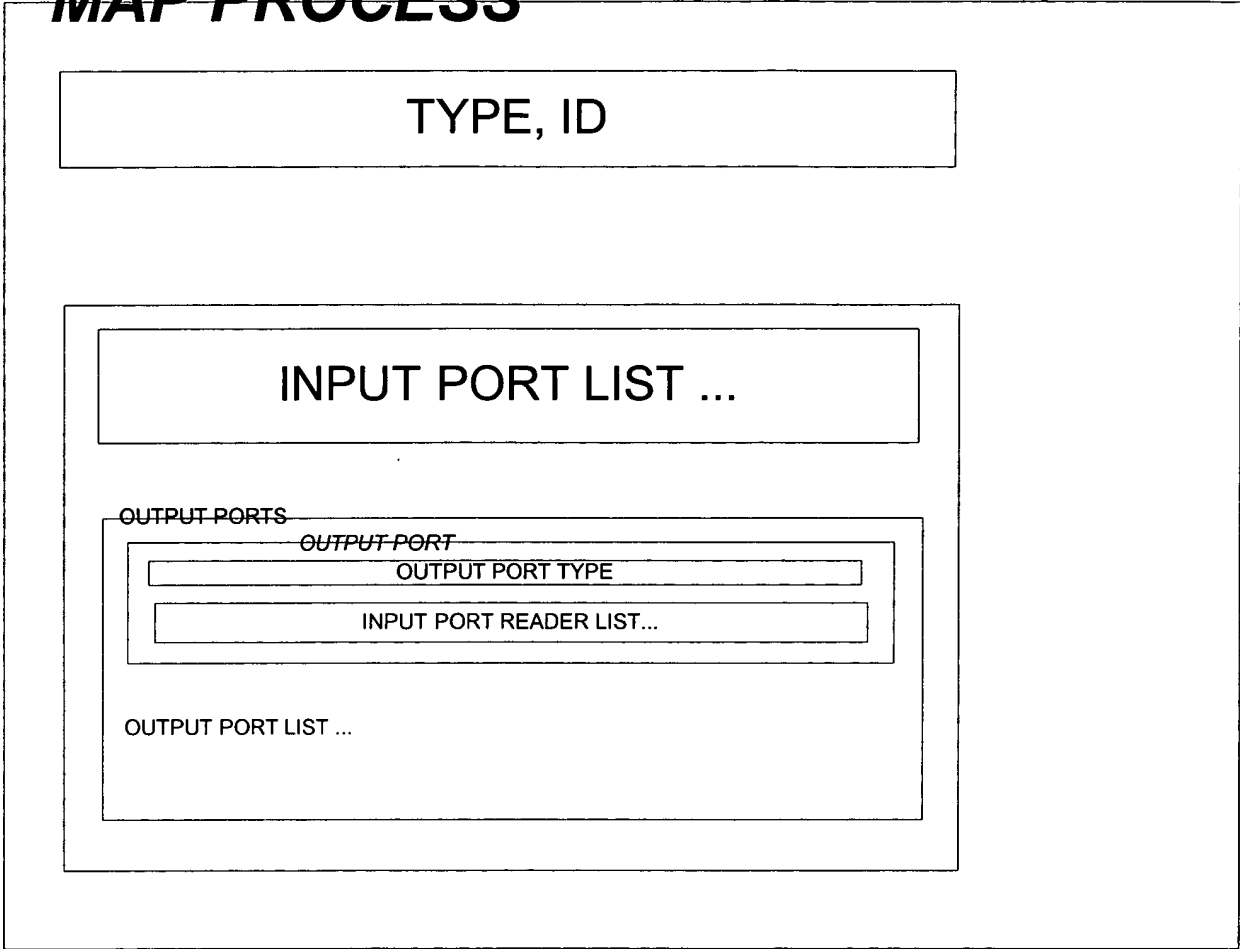
INTERNAL MAP PROCESS INSTANCE  
DECLARATION LIST... (AND CONFIGURATIONS)

PORT TO PORT LINK LIST...

INTERNAL MAP LIST...

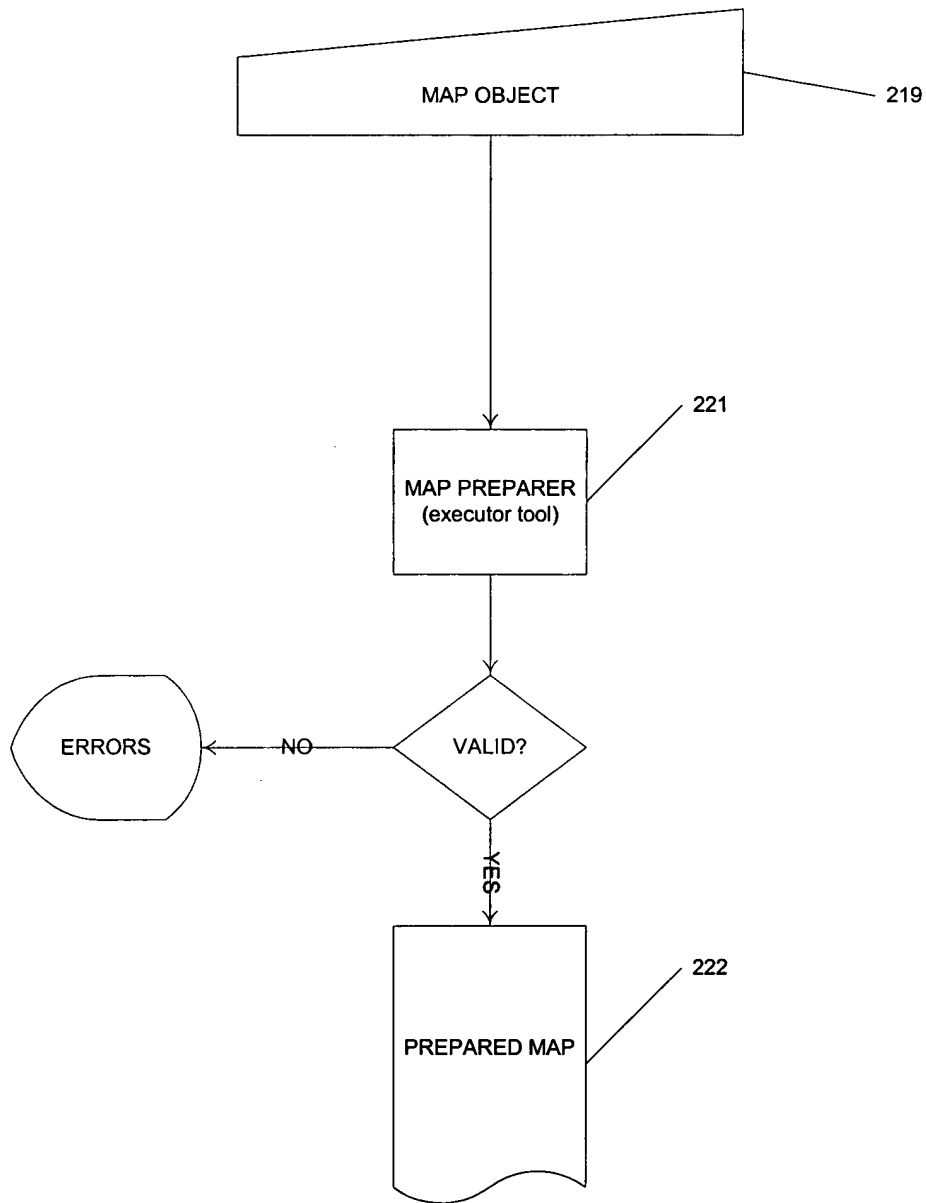
Fig. 12

**MAP PROCESS**



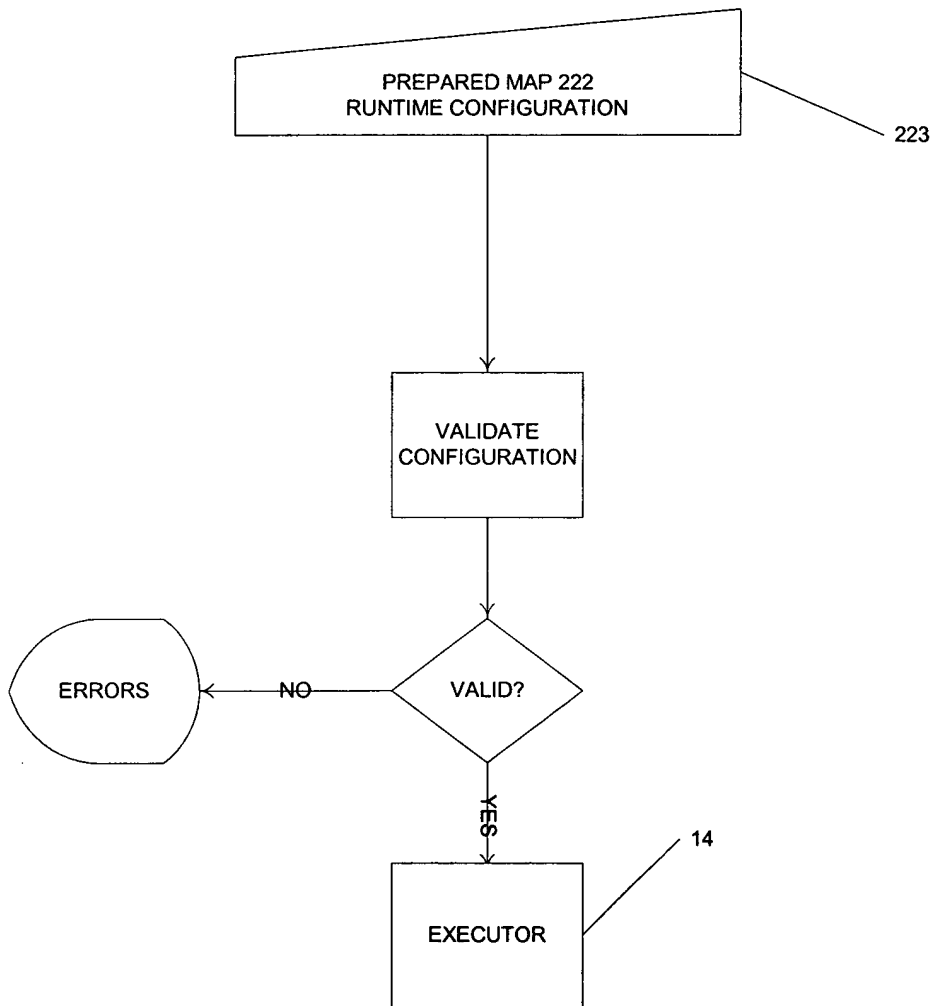
MAP PROCESS LIST ...

# MAP PREPARATION



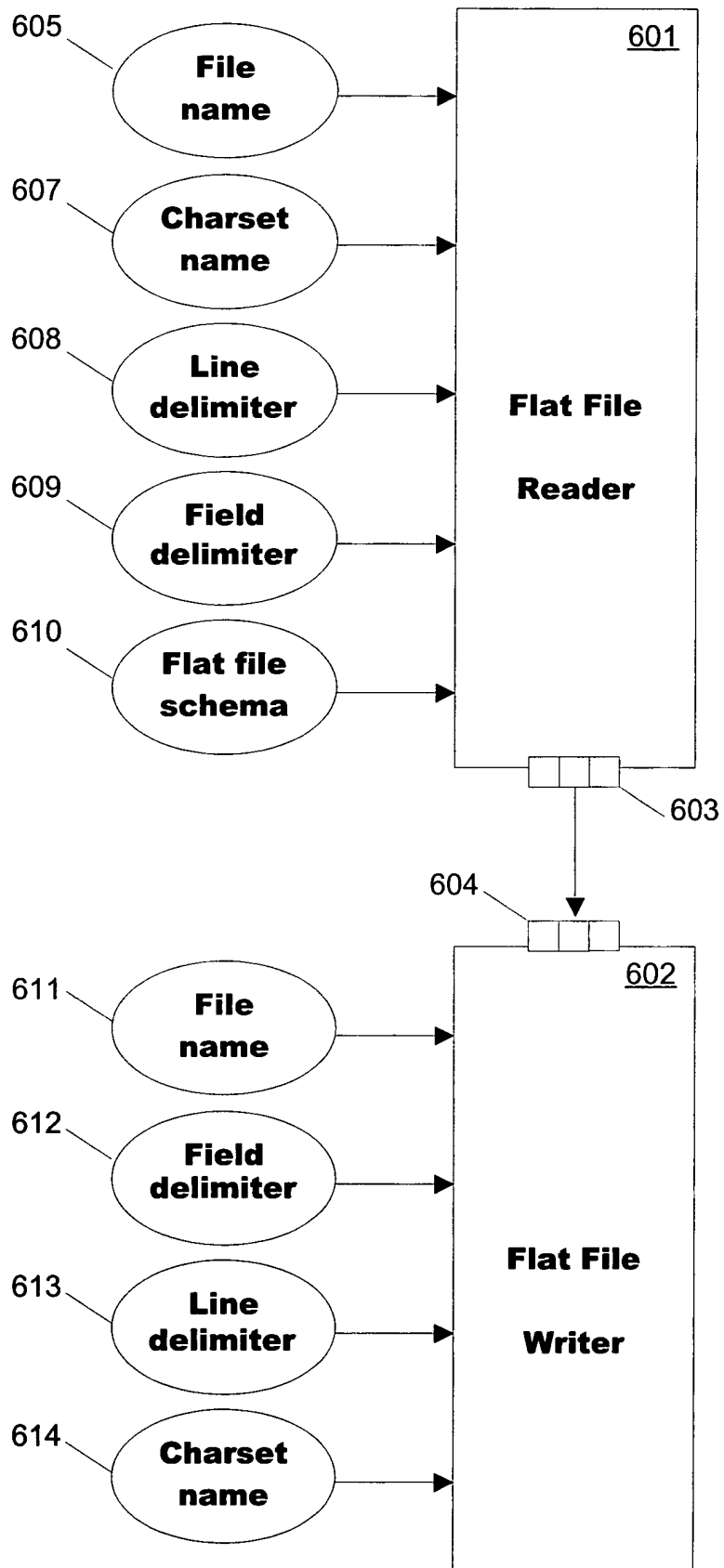
**Fig. 13**

# PREPARED MAP EXECUTION

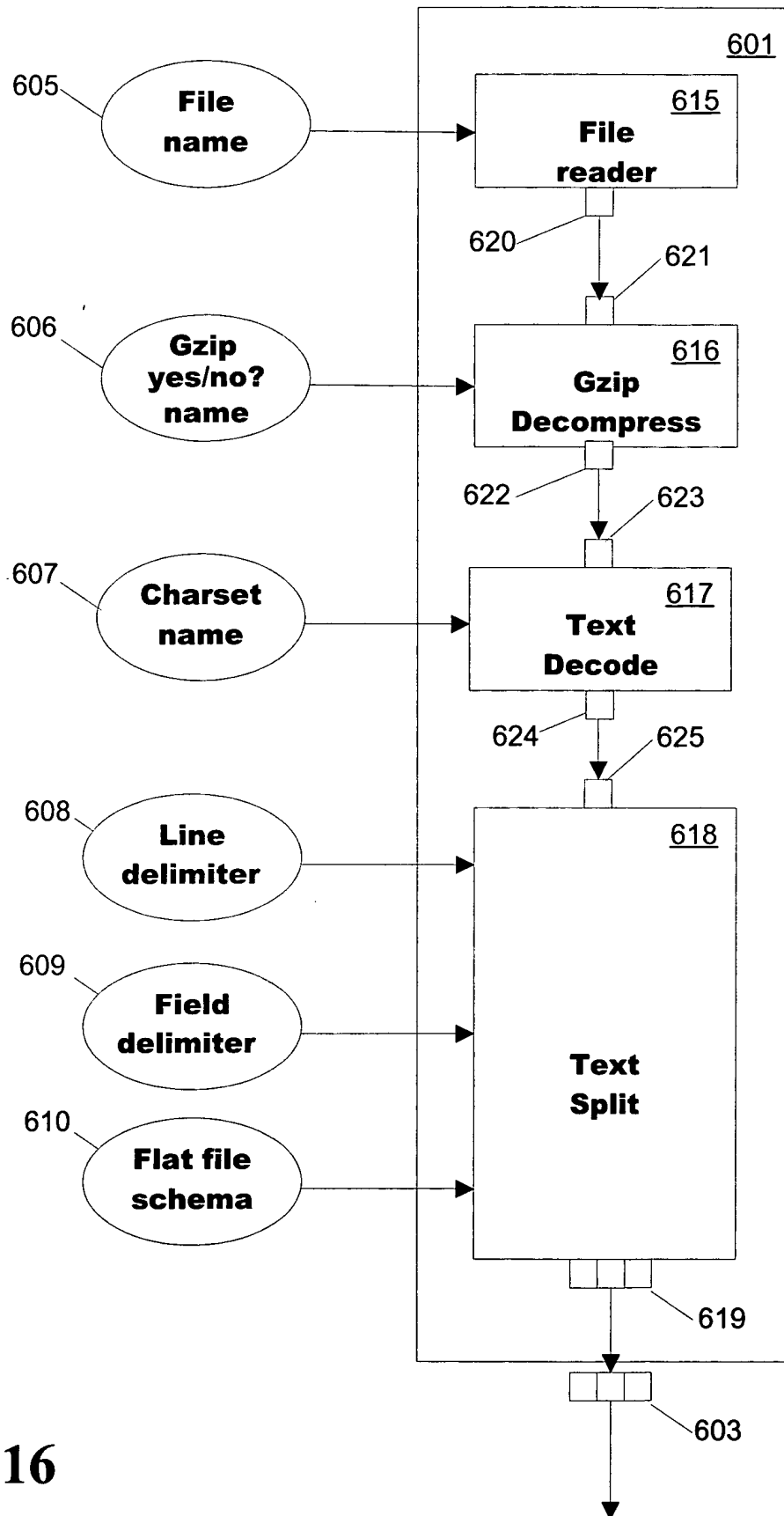


**Fig. 14**

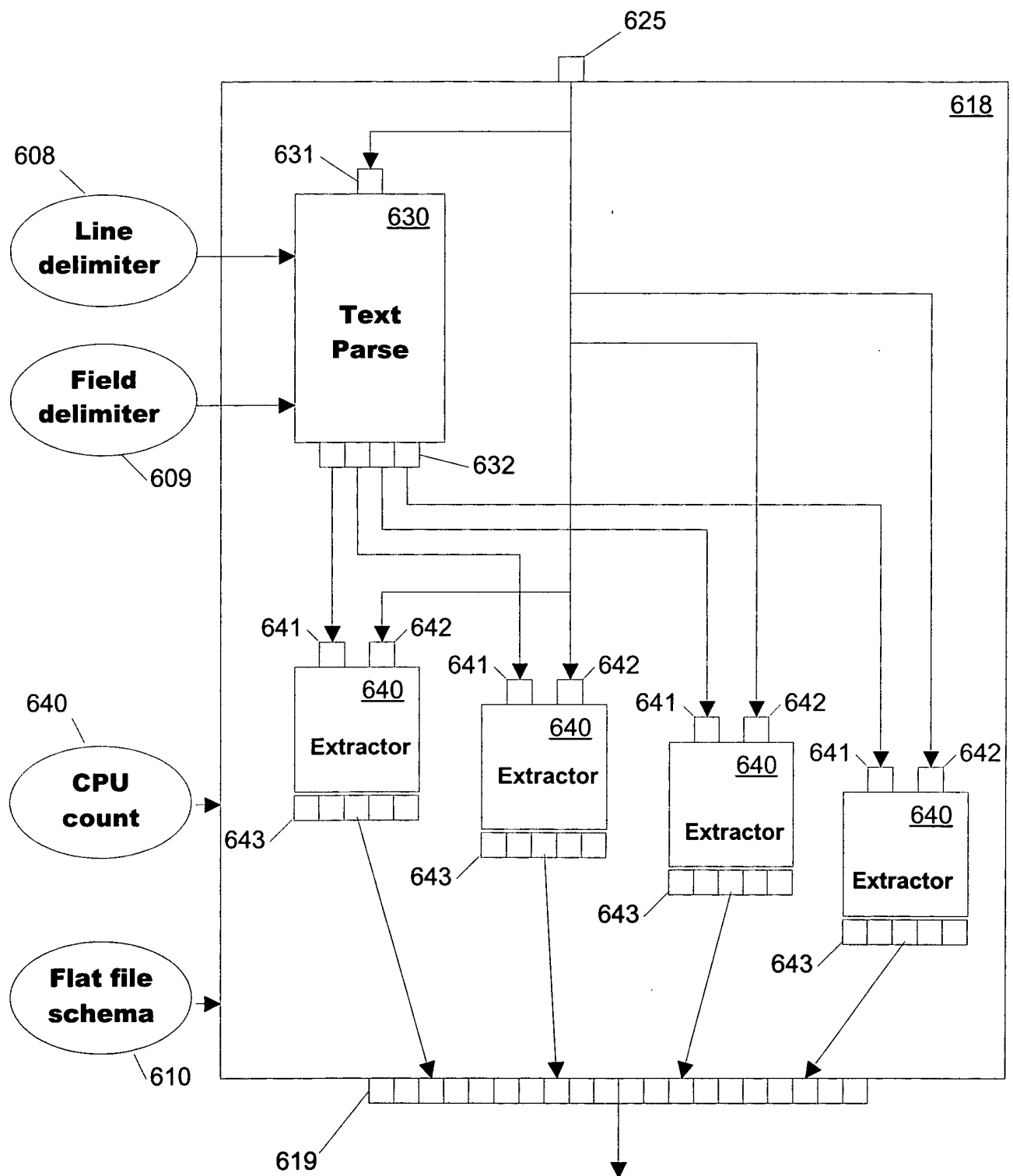




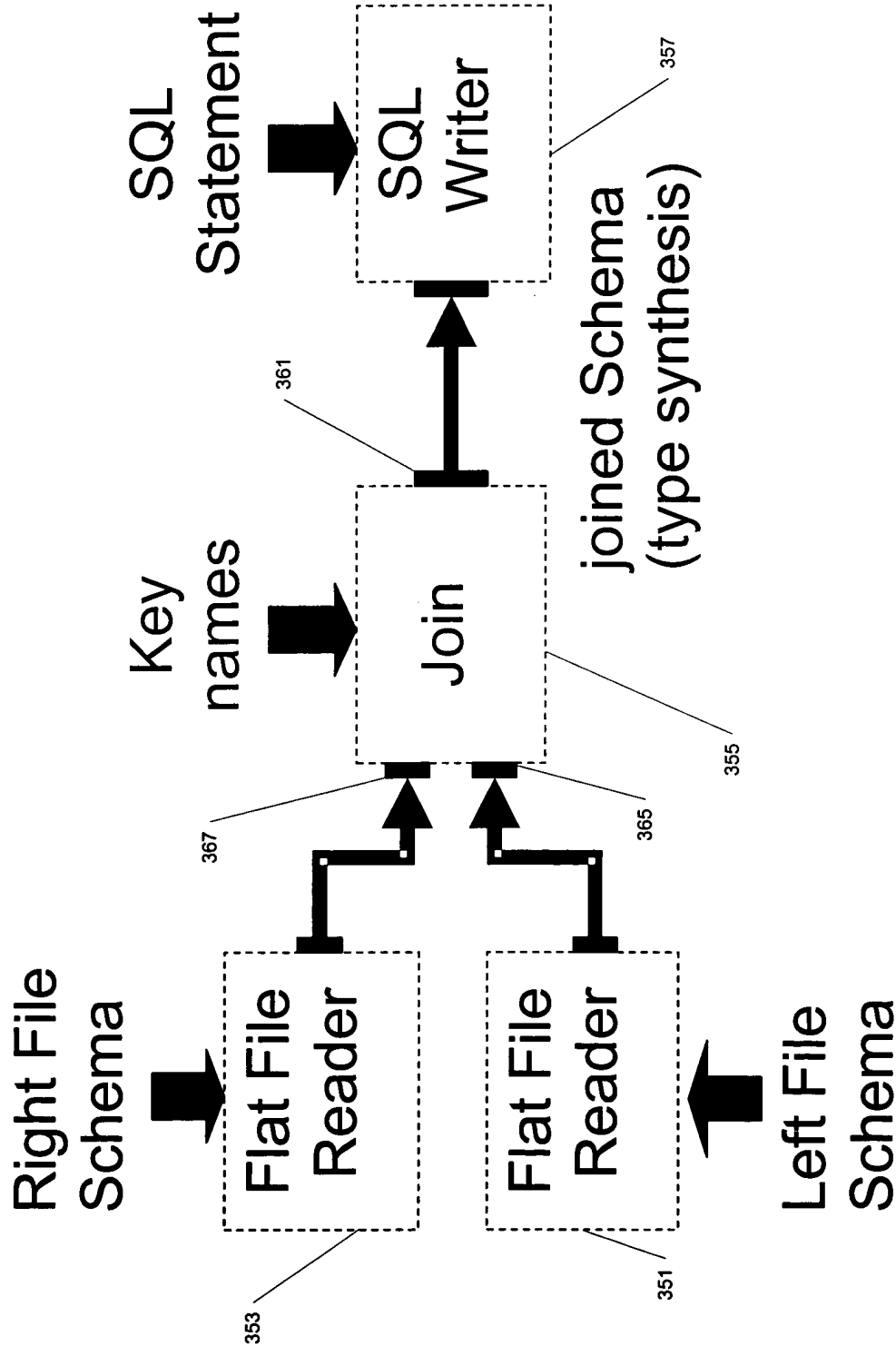
**Fig. 15**



**Fig. 16**



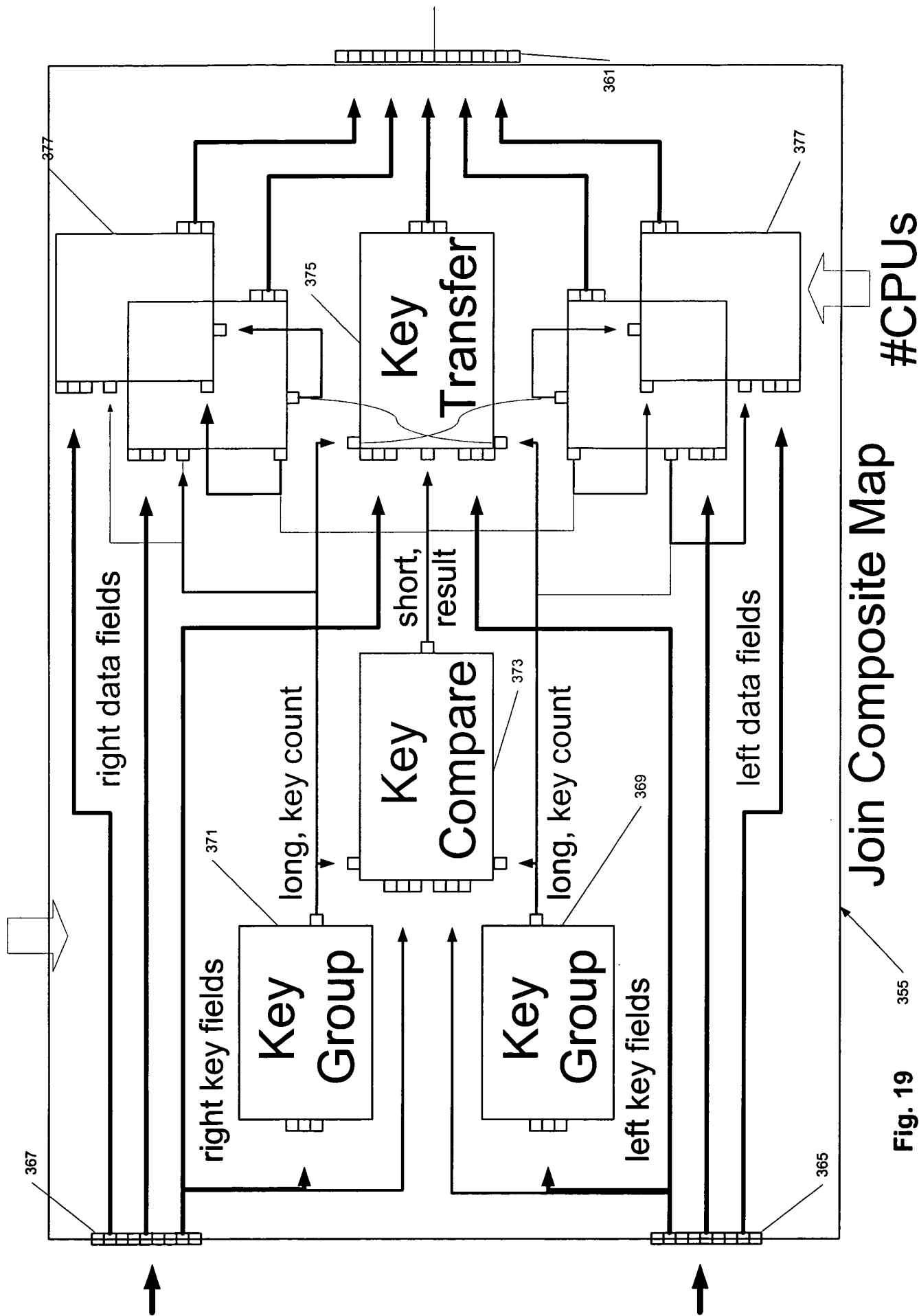
**Fig. 17**



Join Example

Fig. 18

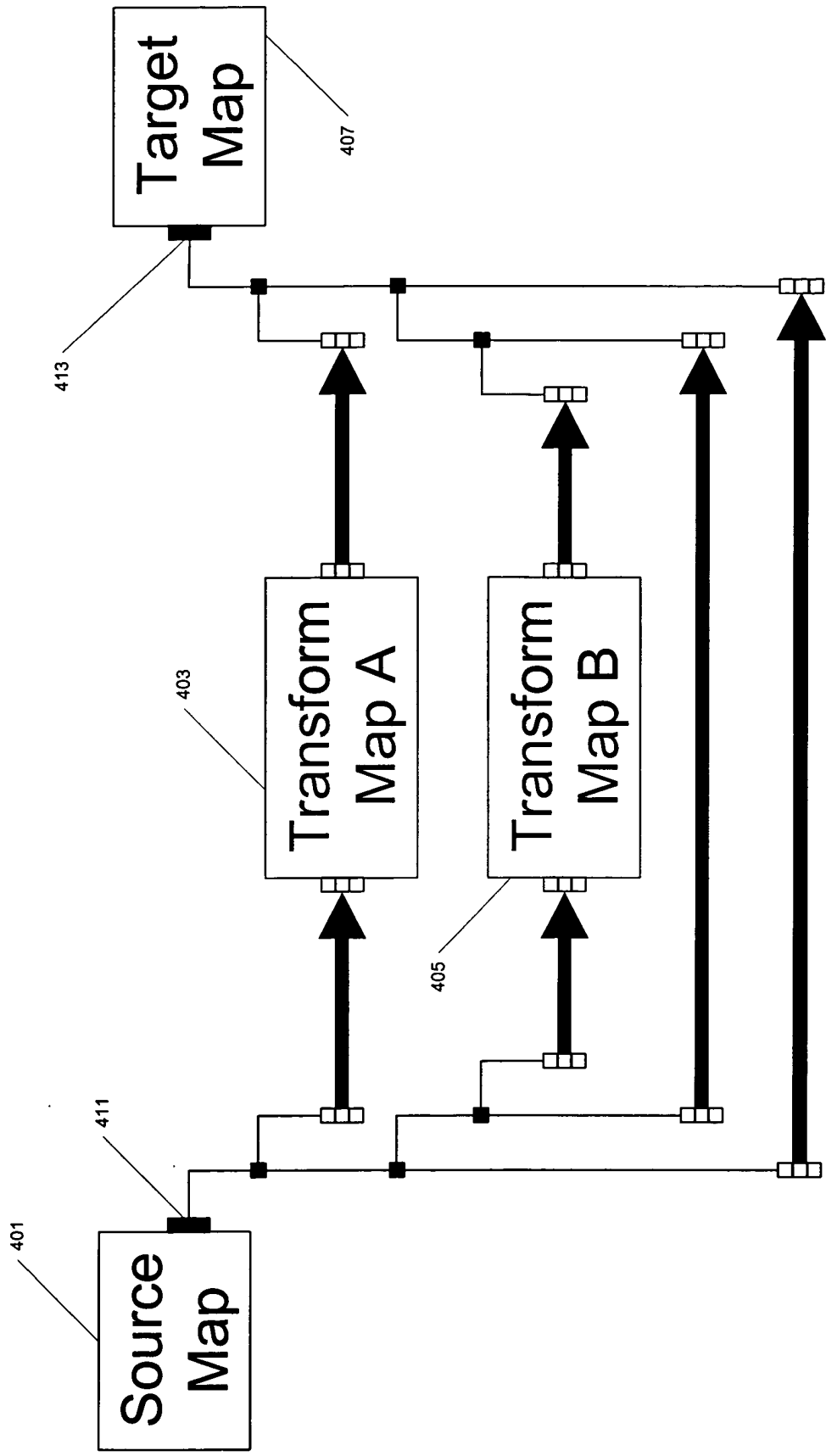
Key names



Join Composite Map

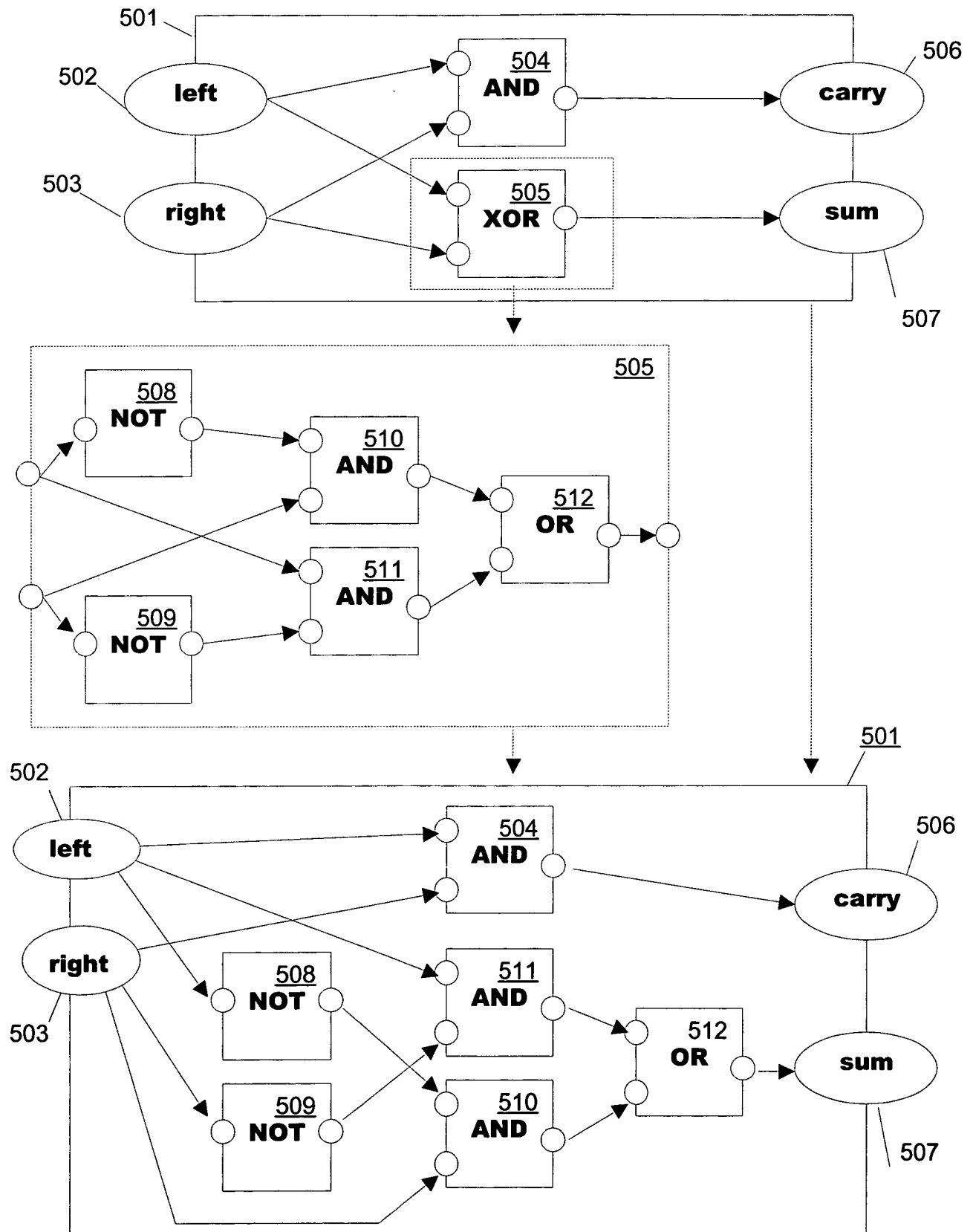
#CPUS

Fig. 19



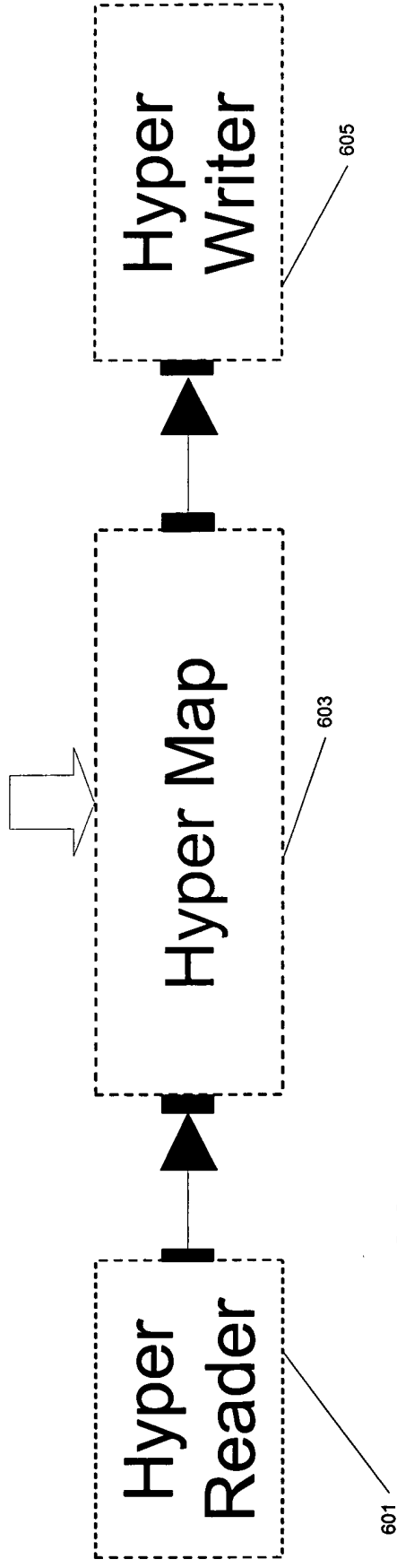
# Hierarchical Composite Ports

Fig. 20



**Fig. 21**

Transformation map  
+ properties



Hyper Map is a Map Template

Fig. 22



Transformation

map  
+ properties

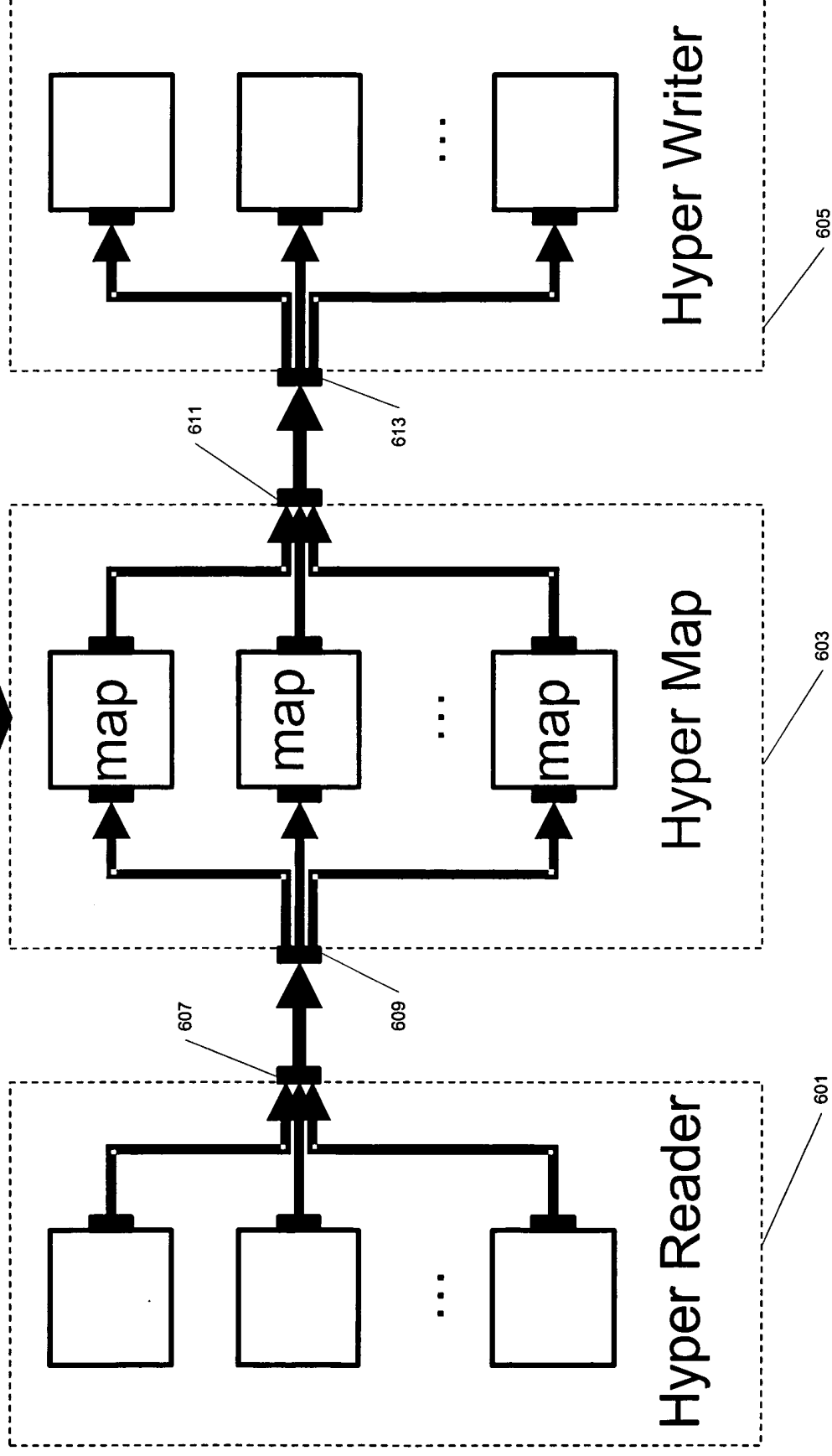


Fig. 23

Hyper Map Implements Partitioned Parallelism

Transformation map  
+ properties

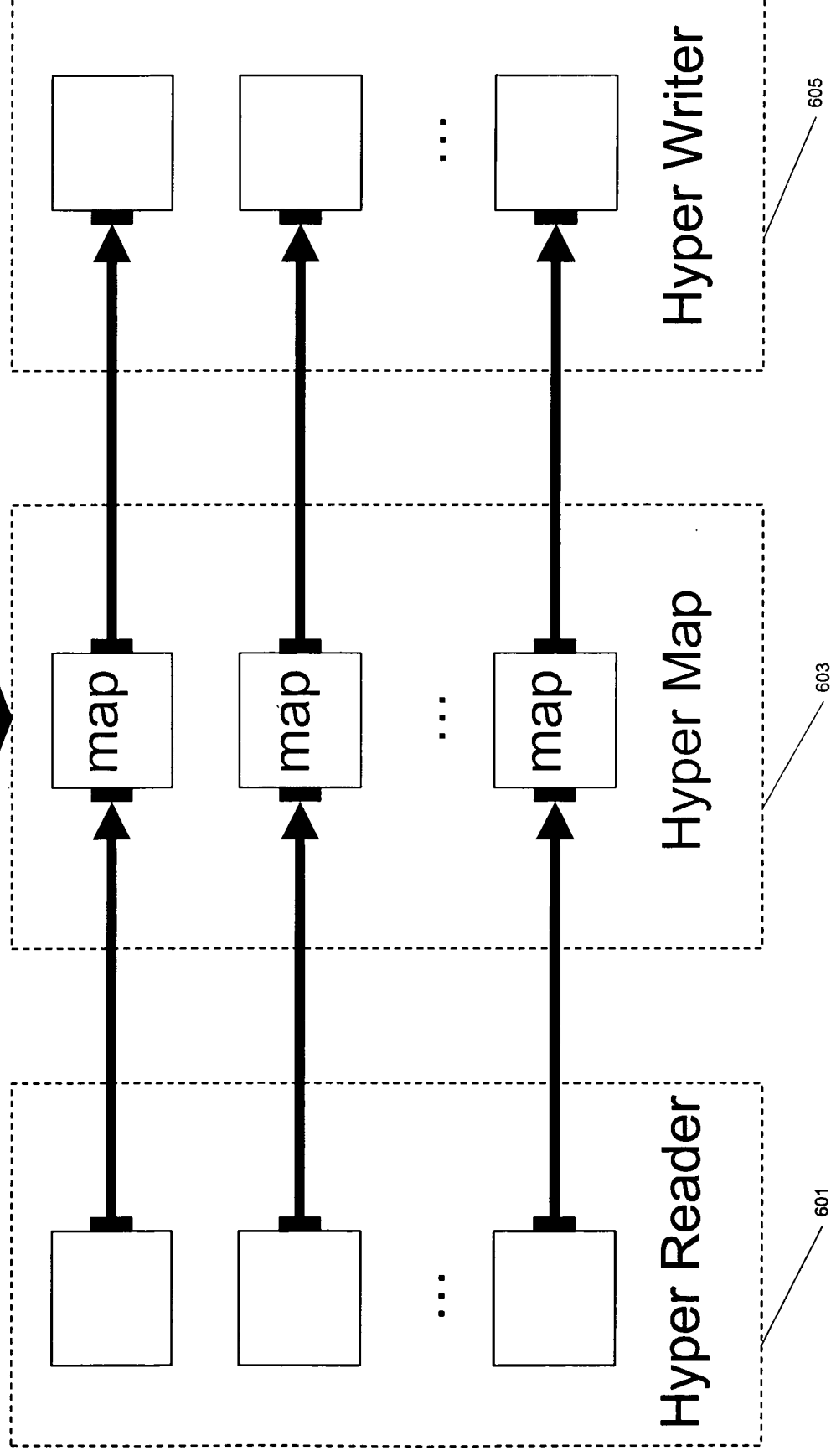


Fig. 24

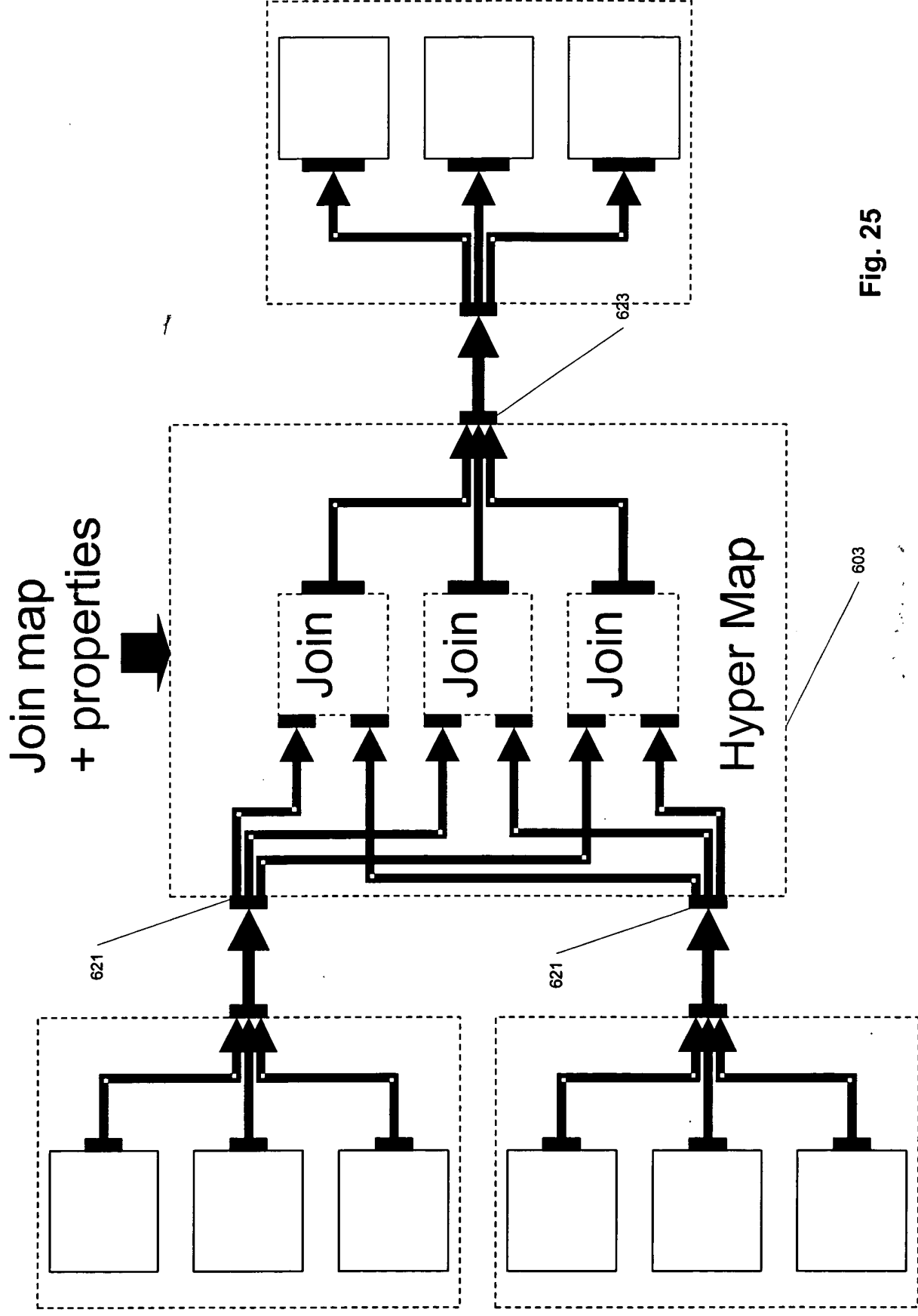


Fig. 25

Hyper Map Partitions another Map's Interface

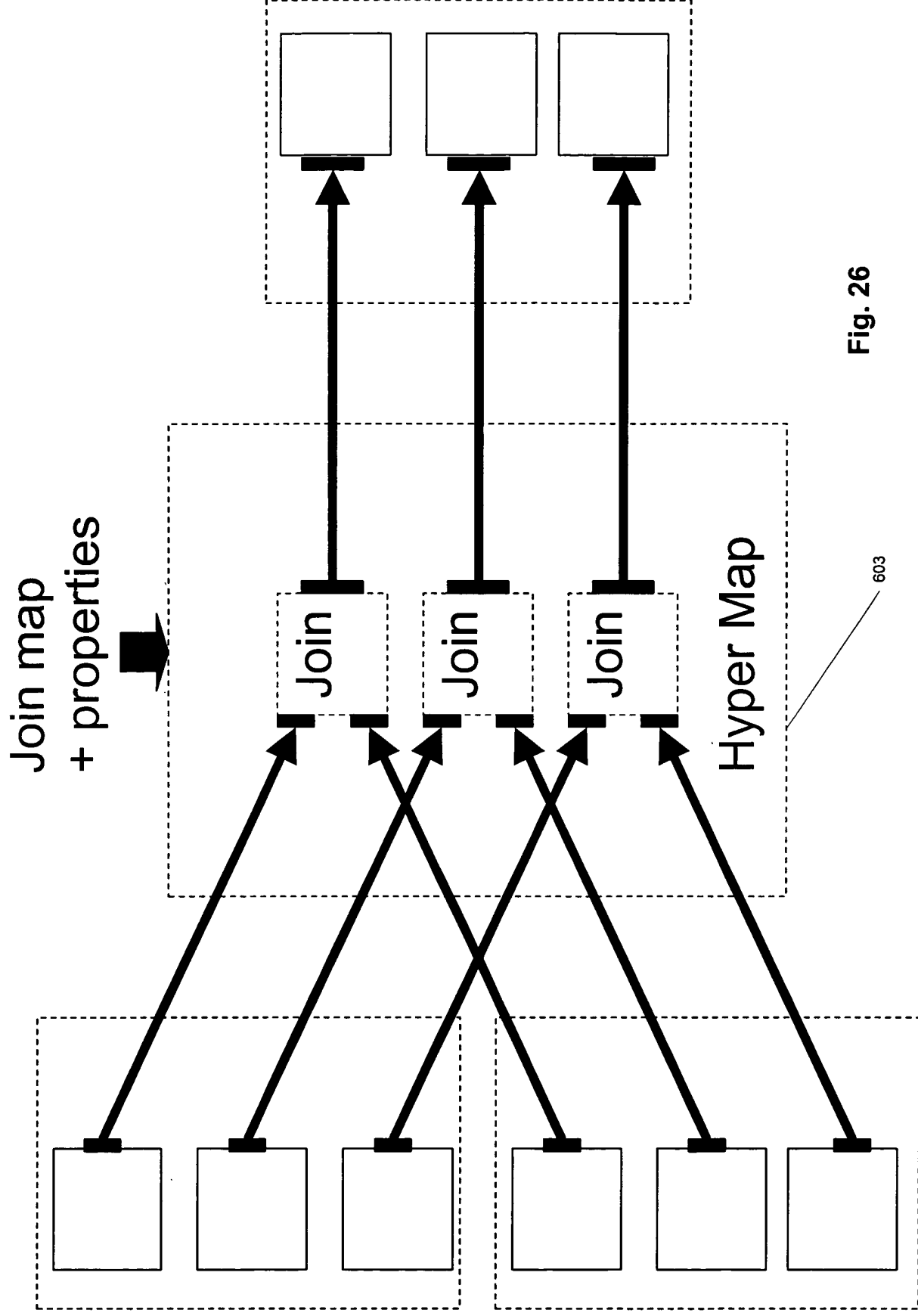


Fig. 26

Hyper Map Implements Partitioned Join

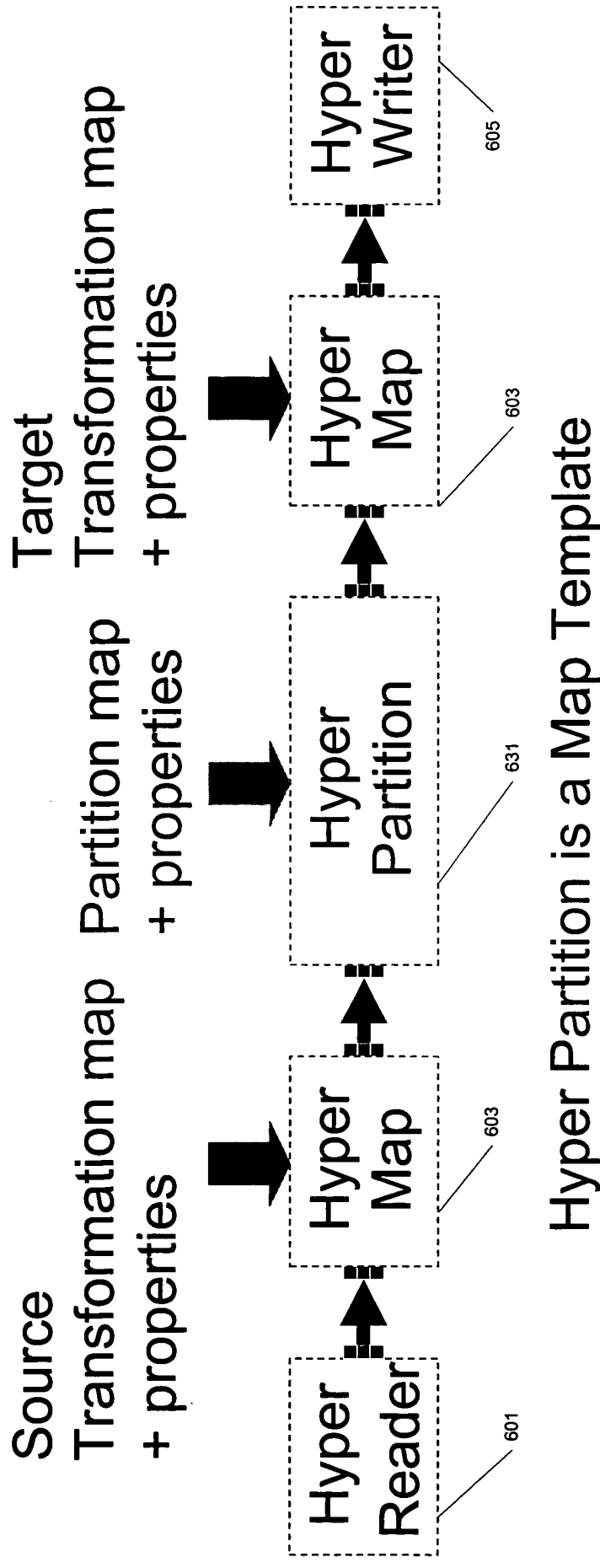
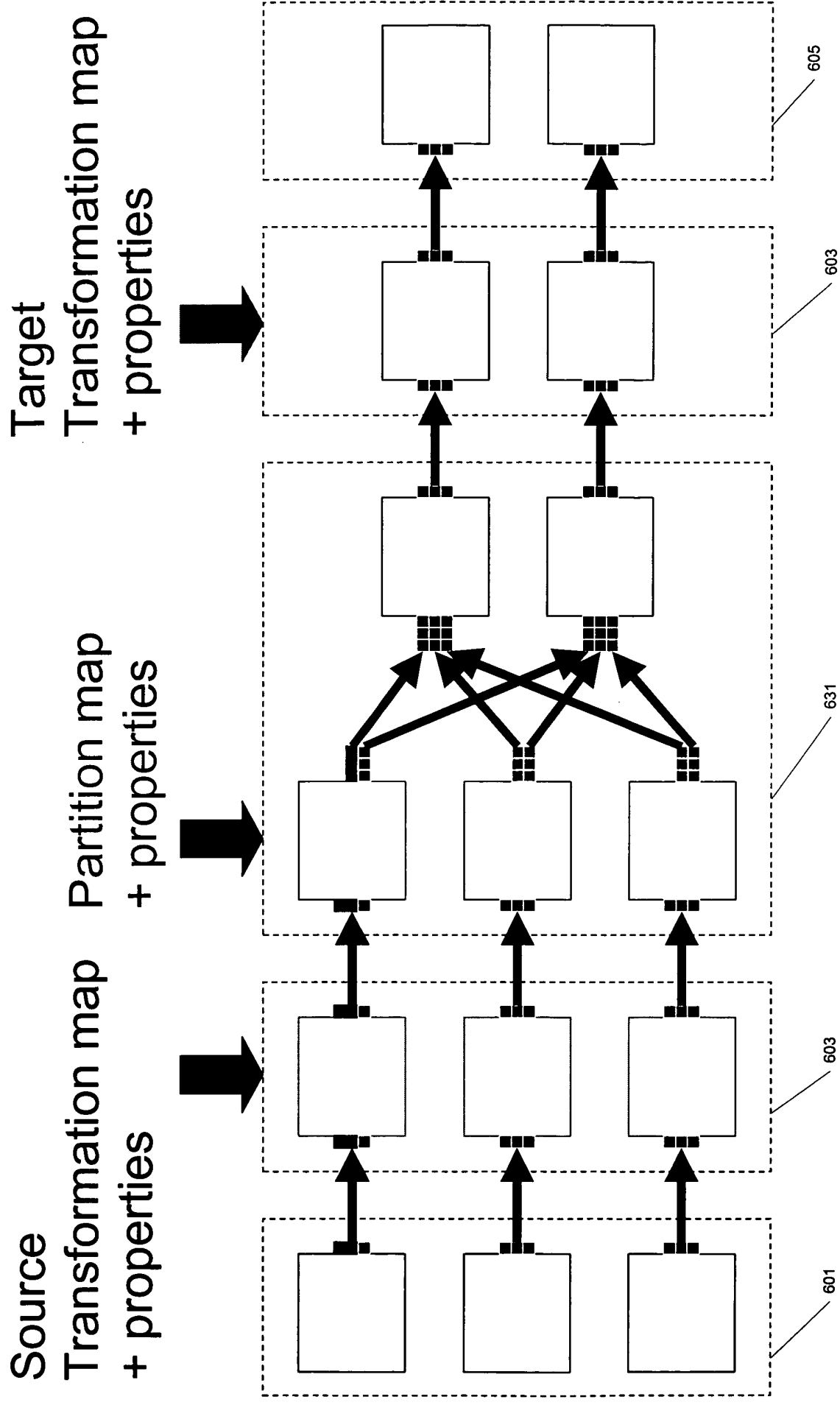


Fig. 27



Hyper Partition corrects Partition Schema Mismatch

Fig. 28

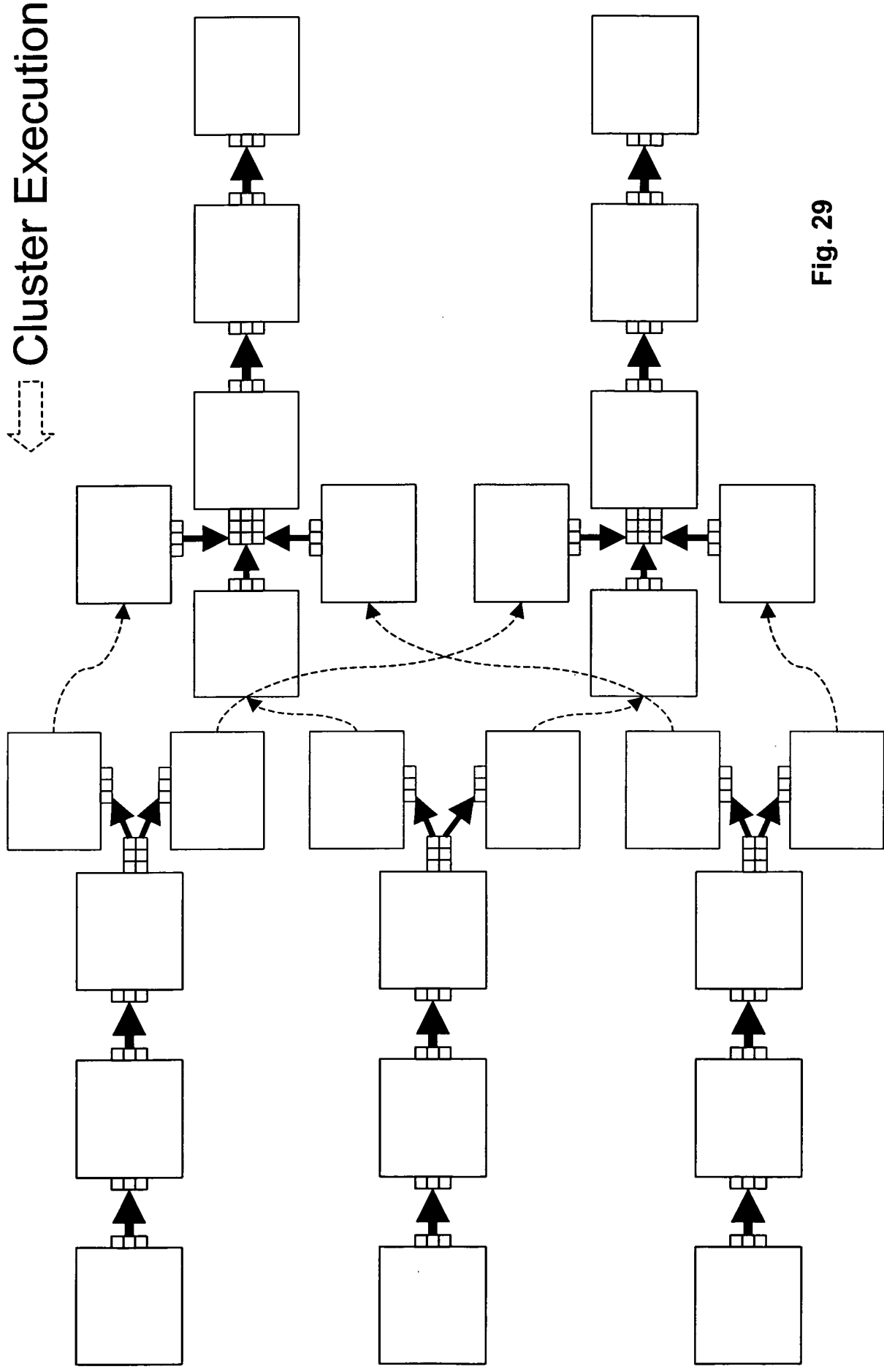


Fig. 29

Cluster Execution of Hyper Partition Pattern

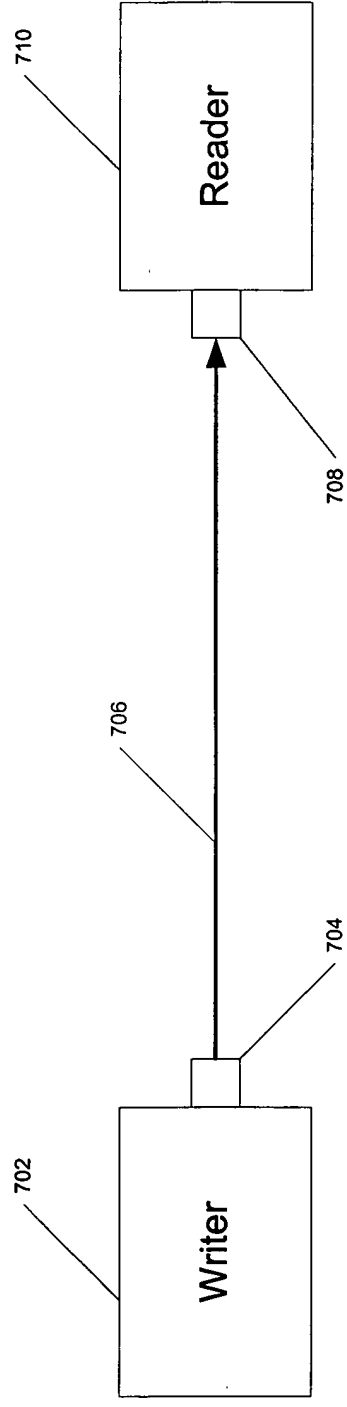


Fig. 30